IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	Ebrahim Andideh et al.	Art Unit:	2811
Serial No.:	10/712,205	Examiner:	Samuel A. Gebremariam
Filed:	November 12, 2003	Atty Docket:	ITL.1008US P15533
For:	Parallel Electrode Memory	Assignee:	Intel Corporation

Mail Stop **Amendment**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF PRIOR INVENTORSHIP

Sir:

We the undersigned inventors hereby declare as follows:

1. We are the inventors of U.S. Patent Application 10/712,205.

2. On or before the filing date of April 2, 2002 of the United States published patent application 2003/0185048, we invented the subject matter of the above-referenced patent application and were diligent to filing a patent application thereon.

3. Namely, on or about January, 2002, we submitted an invention disclosure to obtain a patent application and a true and correct copy of that disclosure is attached hereto.

4. Referring to our claim 1, a first and second layer of memory material spaced from one another in a first direction is shown in that disclosure in Figure 1. There, there are successive polymer layers, polymer 1, polymer 2, polymer 3, all the way up to polymer n, spaced from one another in a first direction which is a vertical direction. Further, the claim calls for in a second address line substantially in said first direction through the first and second layers. The address line is labeled metal 1 in Figure 1.

Therefore, we clearly had conceived of the idea prior to the filing date of the cited reference.

5. We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: 3/27/06

Ebrahim Andideh

Date: 3/22/06

Richard L. Coulson

BOXCAR RELATED – SEND to WIRELESS COMMITEE
TMG INVENTION DISCLOSURE, Rev 1, 2/98
Located at: http://legal.intel.com

24237
P15533

LEGAL ID# _____(legal dept. use only) DATE: Jan. 3, 2002

It is important to provide accurate and detailed information on this form (fill in ALL areas under Inventor[s]). The information will be used to evaluate your invention for possible filing as a patent application. When completed, please return this form to **Janice Boulden, Intel Legal Department at JF3-147. You can submit electronically if all of the information is electronic, including drawings and supervisor approval.** If you have any questions regarding this form or to whom it should be forwarded, please call **503-264-0444**.

Fill out the below and follow the instructions:

1. **Field of the Invention:**
   - ☐ Semiconductor Process: device and integration
   - X Semiconductor Process + Equipment: thin films
   - ☐ Semiconductor Process + Equipment: etch/litho
   - ☐ Circuit Design
   - ☐ Flash
   - ☐ Test
   - ☐ CQN (Q&R)
   - ☐ Packaging
   - ☐ Boards/Cartridge
   - ☐ Automation
   - ☐ Other

2. **Concise Title of Invention:**

   A Novel Ferroelectric Polymer Memory Structure

3. **Brief Description of Invention (please use only space provided and font #10 or larger. Write the Key Elements of the Invention):**

   The invention is :
   Fabrication of horizontal polymer memory cell as shown in Figure 1.

4. Inventor(s):

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Citizenship: USA	Supervisor Name: Chi-Hwa Tsang	Supervisor Phone: 613-7036	Supervisor M/S: RA1-234
Group Name: TMG Division Name: ATD___ PTD_X_ CTM___ CR___	BUM Presenter: Sanjay Panditji	Inventor Signature:	

Inventor Name: Rick Coulson	SS# 522-98-7127	Empl.# 10034900	M/S:JF2-53
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Group Name: TMG Division Name: ATD___ PTD__ CTM___ CR___	BUM Presenter: Sanjay Panditji	Inventor Signature:	

5. ***HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM (use first inventor's supervisor if multiple inventors)***

DATE: Jan . 2002
BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID.

6. **Has subject matter of present disclosure been disclosed or will it be disclosed outside Intel?**
If yes, explain and give date: No
(Give expected tape out date if applicable):

7. **Has the subject matter of present disclosure been published or will it be published outside of Intel?** NO
If yes, explain and give date:

8. **Has a product using or manufactured using the present disclosure been sold or offered for sale?**
If yes, explain and give date: NO

9. **Has this invention been conceived, or constructed during accomplishment of a government or third party contract? If yes, give contract name and number:** NO

10. **Explain the problem being addressed by the invention:**
This invention addresses the problem of:
Fabrication of smaller memory cell to increase the memory density as shown in Figure 1.

11. **Explain current state of the art (i.e., how the problem is solved today):**
Presently the problem described above is solved by
Memory cells are stacked and metal electrodes are located on top and bottom of the polymer memory cells.

State of the Art	**This invention**
Shown in Figure 2, lower density with more complicated integration processes.	Shown in Figure 1, higher density, lower fabrication cost.

12. **Explain technical advantages of the invention over current state of the art:**
The technical advantage of this invention is:

This is a new approach for fabricating polymer memory

13. a. **Is the invention experimentally verified?** No
b. **Is the invention verified with simulation?** N/A
c. **If neither a. or b. above, then you can get a patent on the concept, but please explain the technical basis to justify that your invention will work (use extra space if necessary):**

14. **Detailed Description of Invention (<u>try to use only the space provided</u> with font #10 or larger type. Refer to your drawings):**
Please see Figure 1.

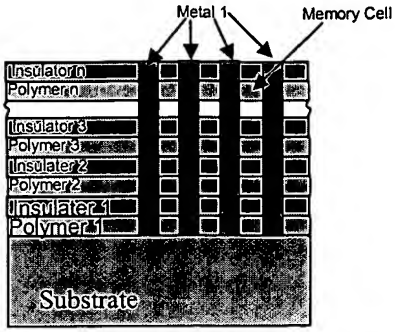

Figure 1. Each metal filled trench is a word line or a bit line.

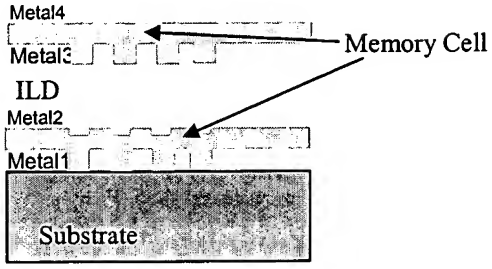

Figure 2. State of the art polymer memory structure.

15. **<u>Referenced sketches/dwg's/diagrams: (use additional page(s))</u>**

16. **Key Supporting Data (1 page limit on separate page):**
This is a Conceptual Invention. We have not fabricated this structure yet.

17. **What is the product or process invention to be used on? (e.g., P8xx, name of product, etc.):**
P822 and future polymer material integration.

18. **Have you reviewed your invention with a TMG Patent Mentor? (see below for mentor names) If so, give name:**